Warning (18236): Number of processors has not been specified which may cause overloading on shared machines. Set the global assignment NUM\_PARALLEL\_PROCESSORS in your QSF to an appropriate value for best performance.

Warning (332068): No clocks defined in design.

Compilation error when elements not connected

Error (10228): Verilog HDL error at eight\_bit\_sub\_add\_structural.v(15): module "eight\_bit\_sub\_add" cannot be declared more than once

// Eight-Bit Sub/Add Test Bench

`timescale 1ns/100ps

module eight\_bit\_sub\_add\_tb;

// internal wires and register declarations

wire [7:0] D\_S;

wire B\_COUT;

reg [7:0] A,B;

reg B\_CIN, SUB\_ADD;

// unit under test

eight\_bit\_sub\_add UUT (.D\_S(D\_S), .B\_COUT(B\_COUT),

.A(A),.B(B), .B\_CIN(B\_CIN),.SUB\_ADD(SUB\_ADD));

initial

begin

// 1) Add no carry on B\_COUT

SUB\_ADD = 0; // Add mode

B\_CIN = 0; // No Carry in

A = 17; // A = 8'b00010001

B = 2; // B = 8'b00000010

// D\_S = A + B = 19 -- 8'b00010011

// 2) Subtract no borrrow on B\_COUT

#100 // 100ns delay

SUB\_ADD = 1; // Subtract mode

B\_CIN = 0; // No Borrow in

A = 17; // A = 8'b00010001

B = 2; // B = 8'b00000010

// D\_S = A - B = 15 -- 8'b00001111

// 3) Add with pending carry on B\_CIN

#100 // 100ns delay

SUB\_ADD = 0; // Add mode

B\_CIN = 1; // Carry in

A = 17; // A = 8'b00010001

B = 2; // B = 8'b00000010

// D\_S = A + B + B\_CIN = 20 -- 8'b00010100

// 4) Subtract with pending borrow on B\_CIN

#100 // 100ns delay

SUB\_ADD = 1; // Subtract mode

B\_CIN = 1; // Borrow in

A = 17; // A = 8'b00010001

B = 2; // B = 8'b00000010

// D\_S = A - B - B\_CIN = 14 -- 8'b00001110

// 5) Add where internal carry propogates from LSB to B\_COUT

#100 // 100ns delay

SUB\_ADD = 0; // Add mode

B\_CIN = 1; // Carry in

A = 253; // A = 8'b11111101

B = 2; // B = 8'b00000010

// D\_S = A + B = 255 + B\_CIN = 256 -- 8'b00000000, B\_COUT = 1

// 6) Subtract where borrow propogates from LSB to borrow request on B\_COUT

#100 // 100ns delay

SUB\_ADD = 1; // Subtract mode

B\_CIN = 1; // Borrow in

A = 2; // A = 8'b00000010

B = 2; // B = 8'b00000010

// D\_S = A - B - B\_CIN = -1 -- 8'b11111111, B\_COUT = 1

// 7) Add that causes an overflow into the carry bit

#100 // 100ns delay

SUB\_ADD = 0; // Add mode

B\_CIN = 0; // No Carry in the input from a previous stage

A = 128; // A = 8'b10000000

B = 128; // B = 8'b10000000

// D\_S = A + B = 256 -- 8'b00000000, B\_COUT = 1

// 8) Subtract larger positive number from smaller positive number

#100 // 100ns delay

SUB\_ADD = 1; // Subtract mode

B\_CIN = 0; // No Borrow in the input from a previous stage

A = 1; // A = 8'b00000001

B = 3; // B = 8'b00000011

// D\_S = A - B = -2 -- 8'b11111110, B\_COUT = 1

end

endmodule